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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,707	11/03/2003	Antonio F. Mondragon-Torres	TI-35731	3525

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EXAMINER	
LEE, SIU M	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
05/24/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com

Office Action Summary	Application No.	Applicant(s)	
	10/699,707	MONDRAGON-TORRES ET AL.	
	Examiner	Art Unit	
	SIU M. LEE	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-9, 12-16, 18-19, 21-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12-16* is/are allowed.

6)☒ Claim(s) *3-9, 18-19, 21-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see page 7-8, filed on 4/30/2010, with respect to the rejections of claims 5, 8, and 18 under double patenting have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Peterzell et al. (US 5,722,063).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 3-8, 18-19, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda (US 5,644,597) in view of Peterzell et al. (US 5,722,063).

(1) Regarding claim 5:

Ueda discloses an apparatus (adaptive equalizer as shown in figure 11) comprising:

two or more adaptive equalizers (the adaptive equalizer in figure 11 comprises decision feedback adaptive equalizer 127 and 133 and linear adaptive equalizer 130 and 136);

a plurality of operational blocks (square error integrating circuit 128 and 134, square error integration circuit 131 and 137, comparator 139 and selecting circuit 140 in figure 11) that interconnect the adaptive equalizers (the comparator 130 and selecting circuit 140 interconnect between the decision feedback adaptive equalizer 127, 133 and linear adaptive equalizer 130, 136 as shown in figure 11);

a first control mechanism (unique word of the received signal (11 of figure 16) from received signal memory 110 and 117 in figure 11) that configures the adaptive equalizers according to different signal delay profiles (the training of the equalizers for setting up the taps in the decision feedback adaptive equalizer 127 and 133 and the taps in the linear adaptive equalizer 130 and 136 based on the received unique word (UW) that indicate the propagation characteristic of channel, column 35, lines 18-44) and the plurality of operational blocks (the comparator 139 compares the results outputted from the equalized square error integrating circuit 128, the equalized square error integrating circuit 131, the equalized square error integrating circuit 134 and the equalized square error integrating circuit 137. Next, the comparator 139 selects the adaptive equalizer which is expected to have the minimum sum of equalized square errors, column 36, lines 6-12, as the equalized square error is also depend on the training of the equalizers based on the UW, therefore, the examiner interprets the comparator 139 and selecting circuit 140 also being configured by the received UW that is received and affected by the characteristics of the channel);

a third control mechanism that disables a computation resource of at least one of said adaptive equalizers according to the different signal delay profiles (the comparator

124 outputs the result of selection to the selecting circuit 140 and outputs a stop signal to each of the remaining three adaptive equalizers which have not been selected, these adaptive equalizers stop the equalization of the remaining random data corresponding to the same burst in response to the stop signal, column 36, lines 14-19; the examiner interprets stopping the equalization process as disable the equalizer, as the claim does not specified the claimed computation resource is not included in the equalizer, the examiner interprets the computation resource is the computation resource within the equalizer as shown in figure 15, by stopping the equalization process, the computation resource of the equalizer will also be disable).

Ueda discloses selecting an equalizer in a receiving branch based on the comparison by comparator 124 and stop the equalization of three equalizer (column 36, lines 13-19) but fail to explicitly disclose a second control mechanism that disables at least one of said plurality of operational blocks (square error integration circuit 128, 134, and square error integrating circuit 131, 137) according to the different signal delay profiles.

However, Peterzell teaches to power down a device when the device is not in use (bypasses) by a controller in order to reduce power consumption (column 7, liens 39-46).

It is desirable to employ the teaching Peterzell in the apparatus of Ueda to have a second control mechanism that disables at least one of said plurality of operational blocks (the square error integration circuit 128, 134, and square error integrating circuit 131, 137 that are not selected based on the comparison in comparator 124) according

to the different signal delay profiles because it will reduce power consumption on the apparatus for powering down the circuit that is not needed. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to power down inactive circuit (the square error integration circuit 128, 134, and square error integrating circuit 131, 137 that are not selected) as taught by Peterzell in the apparatus of Ueda to reduce power consumption of the apparatus.

(2) Regarding claim 3:

Ueda further discloses that wherein each of said two or more adaptive equalizer comprises a computation resource (figure 15 shows the detail of a conventional adaptive equalizer with at least a tap coefficient update circuit (column 20, lines 40-51)).

(3) Regarding claim 4:

Ueda further discloses wherein the computation resource comprises at least one item selected from the group consisting of: a summer, a conjugate block; a multiplier, and a divider (figure 15 shows an adder 5 and multiplier in block 2).

(4) Regarding claim 6:

Ueda further discloses wherein said operational blocks comprise at least one item from the group consisting of: a signal generator, a delay line, and a summer (the examiner interpret the square error integrating circuit 128 and 134 as a signal generator for generating the integration of the squared equalized error for each antenna branch, column 46, lines 2-6).

(5) Regarding claim 7:

Ueda further disclose wherein the different signal delay profiles comprise at least one multi-path signal profile selected from the group consisting of:

sub-signals that arrive to the apparatus in consecutive chip time units;

sub-signals wherein one sub-signal comprises a substantial amount of total energy of the sub-signals;

sub-signals that do not arrive to the apparatus in consecutive chip time units;

sub-signals that arrive to the apparatus in two or more clusters (the delay time of the delay wave is less than or equal to 0.35 symbol or the delay time of the delay wave is more than 0.35 symbol, column 46, line 64 – column 47, line 3); and

sub-signals that arrive to the apparatus from more than one antenna.

(6) Regarding claim 8:

Ueda discloses an apparatus (adaptive equalizer as shown in figure 11) comprising:

two or more adaptive equalizers (the adaptive equalizer in figure 11 comprises decision feedback adaptive equalizer 127 and 133 and linear adaptive equalizer 130 and 136);

a plurality of operational blocks (square error integrating circuit 128 and 134, square error integration circuit 131 and 137, comparator 139 and selecting circuit 140 in figure 11) that interconnect the adaptive equalizers (the comparator 130 and selecting circuit 140 interconnect between the decision feedback adaptive equalizer 127, 133 and linear adaptive equalizer 130, 136 as shown in figure 11);

a first control mechanism (unique word of the received signal (11 of figure 16) from received signal memory 110 and 117 in figure 11) that configures the adaptive equalizers (the training of the equalizers for setting up the taps in the decision feedback adaptive equalizer 127 and 133 and the taps in the linear adaptive equalizer 130 and 136 based on the received unique word (UW) that indicate the propagation characteristic of channel, column 35, lines 18-44) and the plurality of operational blocks according to different signal delay profiles (the training of the equalizers for setting up the taps in the decision feedback adaptive equalizer 127 and 133 and the taps in the linear adaptive equalizer 130 and 136 based on the received unique word (UW) that indicate the propagation characteristic of channel, column 35, lines 18-44) and the plurality of operational blocks (the comparator 139 compares the results outputted from the equalized square error integrating circuit 128, the equalized square error integrating circuit 131, the equalized square error integrating circuit 134 and the equalized square error integrating circuit 137. Next, the comparator 139 selects the adaptive equalizer which is expected to have the minimum sum of equalized square errors, column 36, lines 6-12, as the equalized square error is also depend on the training of the equalizers based on the UW, therefore, the examiner interprets the comparator 139 and selecting circuit 140 also being configured by the received UW that is received and affected by the characteristics of the channel); and

a third control mechanism that disables a computation resource of at least one of said adaptive equalizers according to the different signal delay profiles (the comparator 124 outputs the result of selection to the selecting circuit 140 and outputs a stop signal

to each of the remaining three adaptive equalizers which have not been selected, these adaptive equalizers stop the equalization of the remaining random data corresponding to the same burst in response to the stop signal, column 36, lines 14-19; the examiner interprets stopping the equalization process as disable the equalizer, as the claim does not specified the claimed computation resource is not included in the equalizer, the examiner interprets the computation resource is the computation resource within the equalizer as shown in figure 15, by stopping the equalization process, the computation resource of the equalizer will also be disable); and the first and third control mechanisms comprise multiplexers that receive control signal according to the different signal delay profiles (it is well known in the art that a switch, a selector, or a multiplexer all provide a same function of selecting as evidence by Martinian et al. (US 2003/0101408), paragraph 0053, therefore, the examiner interprets a selecting function would inherently a device that is function equivalent to a multiplexer) (with respect to the first control mechanism, figure 17 discloses using a switch 15 to select one of a two equalizer according to a control signal from switch controller 16 as shown in figure 17; the examiner interpret a switch is functional equivalent to a multiplexer, with respect to the second control mechanism, it involve the selecting of the equalizer with a smaller equalized square errors, the examiner interprets the selecting process would inherently a device that is function equivalent to a multiplexer).

Ueda discloses selecting an equalizer in a receiving branch based on the comparison by comparator 124 and stop the equalization of three equalizer (column 36, lines 13-19) but fail to explicitly disclose a second control mechanism that disables at

least one of said plurality of operational blocks according to the different signal delay profiles and multiplexers that receive control signal.

However, Peterzell teaches to power down a device when the device is not in use (bypasses) by a controller in order to reduce power consumption by connecting the power pin to a switch that is also controlled by the controller (column 7, lines 39-46, the examiner interprets the controlling of the power pin can be perform by a controlled switch which is functional equivalent to a multiplexer, since the claim does not specify each of the first, second and third control mechanism comprises multiplexers, the rejection discloses first and third control mechanism comprises multiplexer, thus satisfied the limitation).

It is desirable to employ the teaching Peterzell in the apparatus of Ueda to have a second control mechanism that disables at least one of said plurality of operational blocks according to the different signal delay profiles because it will reduce power consumption on the apparatus for powering down the circuit that is not needed. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to power down inactive circuit (delay measuring circuit of the non-selected branch of the receiver) as taught by Peterzell in the apparatus of Ueda to reduce power consumption of the apparatus.

(7) Regarding claim 18:

Ueda discloses a system (adaptive equalizer as shown in figure 11) comprising:

two or more adaptive equalizers (the adaptive equalizer in figure 11 comprises decision feedback adaptive equalizer 127 and 133 and linear adaptive equalizer 130 and 136);

a plurality of operational blocks (square error integrating circuit 128 and 134, square error integration circuit 131 and 137, comparator 139 and selecting circuit 140 in figure 11) that interconnect the adaptive equalizers (the comparator 130 and selecting circuit 140 interconnect between the decision feedback adaptive equalizer 127, 133 and linear adaptive equalizer 130, 136 as shown in figure 11);

a means for selectively interconnecting the two or more adaptive equalizers and the plurality of operational blocks according to attributes of a signal profile (the comparator 139 compares the results outputted from the equalized square error integrating circuit 128, the equalized square error integrating circuit 131, the equalized square error integrating circuit 134 and the equalized square error integrating circuit 137. Next, the comparator 139 selects the adaptive equalizer which is expected to have the minimum sum of equalized square errors, column 36, lines 6-12), and the means for selectively interconnecting comprises a multiplexer (it is well known in the art that a switch, a selector, or a multiplexer all provide a same function of selecting as evidence by Martinian et al. (US 2003/0101408), paragraph 0053, therefore, the examiner interprets a selecting function would inherently a device that is function equivalent to a multiplexer) (with respect to the first control mechanism, figure 17 discloses using a switch 15 to select one of a two equalizer according to a control signal from switch controller 16 as shown in figure 17; the examiner interpret a switch is functional

equivalent to a multiplexer, with respect to the second control mechanism, it involve the selecting of the equalizer with a smaller equalized square errors, the examiner interprets the selecting process would inherently a device that is function equivalent to a multiplexer); and

a means for disabling a computational resource of at least one of the two or more adaptive equalizers according to said attributes of signal profile (the comparator 124 outputs the result of selection to the selecting circuit 140 and outputs a stop signal to each of the remaining three adaptive equalizers which have not been selected, these adaptive equalizers stop the equalization of the remaining random data corresponding to the same burst in response to the stop signal, column 36, lines 14-19; the examiner interprets stopping the equalization process as disable the equalizer, as the claim does not specified the claimed computation resource is not included in the equalizer, the examiner interprets the computation resource is the computation resource within the equalizer as shown in figure 15, by stopping the equalization process, the computation resource of the equalizer will also be disable) (as the claim does not specified a computation resource is not included in the equalizer, the examiner interprets the computation resource is the computation resource within the equalizer as shown in figure 15, by deactivating the equalizer, the computation resource of the equalizer will also be deactivate).

Ueda fail to explicitly disclose the means for selectively interconnecting and the means for disabling comprising a multiplexer.

However, Peterzell teaches to power down a device when the device is not in use (bypasses) by a controller in order to reduce power consumption by connecting the power pin to a switch that is also controlled by the controller (column 7, lines 39-46, the examiner interprets the controlling of the power pin can be perform by a controlled switch which is functional equivalent to a multiplexer).

It is desirable to employ the teaching Peterzell in the apparatus of Ueda to have the means for selectively interconnecting and the means for disabling comprising a multiplexer because it will reduce power consumption on the apparatus for powering down the circuit that is not needed. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to power down inactive circuit (delay measuring circuit of the non-selected branch of the receiver) as taught by Peterzell in the apparatus of Ueda to reduce power consumption of the apparatus.

(8) Regarding claim 19:

Ueda fail to explicitly disclose a means for disabling at least one of the plurality of operational blocks according to said attributes of the signal profile.

However, Ueda discloses stop the equalization process of the three non-selected equalizer (column 36, lines 13-19). Therefore, it would have been obvious for Ueda to deactivate the square error integrating circuit and square error integrating circuit of the non-selected equalizer . Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the invention of Ueda to deactivate the error integrating circuit of the non-selected branch as taught by the instant application in order to reduce power consumption.

(9) Regarding claim 22:

Ueda further discloses wherein the attributes of the signal profile comprise at least one selected from the group consisting of:

a number of antennas that transmitted the multi-path signal;

a length of the multi-path signal profile (delay measurement circuit read a receive signal from receive signal memory for measuring a multi-path propagation characteristics on a channel (if the delay time of the delay wave is less than or equal to 0.35 symbol or the delay time of the delay wave is more than 0.35 symbol, column 46, line 64 – column 47, line 3));

an amount of energy in a single sub-signal of the multi-path signal;

an amount of capturable energy by a number of adaptive equalizer; and

a number of energy clusters.

4. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda (US 5,644,597) in view of Peterzell et al. (US 5,722,063) as applied to claim 5 above, and further in view of Yang (US 6,763,074 B1)

Ueda and Peterzell disclose all the subject matter as discuss in claim 5 except wherein a two- stage configuration of the apparatus comprises a default mode.

However, Yang discloses wherein a two-stage configuration of the apparatus comprises a default mode (step 1600 in figure 16, the default mode is selected from a plurality of possible modes of operation, column 10, lines 17-20).

It is desirable wherein a two-stage configuration of the apparatus comprises a default mode because at least the output of a detector appears at the output of the multiplexer and if the same detector is selected, the system can continue with the pre-selected default detector (column 1, line 65 - column 2, line 5). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Yang in the apparatus of Ueda and Peterzell to provide a more efficient system.

5. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda (US 5,644,597) in view of Peterzell et al. (US 5,722,063) as applied to claim 18 above, and further in view of Juan (US 5,642,382).

Ueda and Peterzell discloses all the subject matter as discussed in claim 18 except the system further comprising means for sharing computational resources of the two or more adaptive equalizers.

However, Juan discloses a system that share a single set of arithmetic operators between filters of the equalizers (column 2, lines 4-10).

It is desirable to share computational resources of the two or more adaptive equalizers because it can reduce hardware requirement and lower production cost (column 2, lines 4). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Juan in the system of Ueda and Peterzell to lower the production cost.

Allowable Subject Matter

6. Claims 12-16 are allowed.

7. Claims 3-4, 6-7, 9, 19, 21-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 12-16:

The present invention describes a method comprising receiving a multi-path signal profile; determining attributes of the multi-path signal profile, comprising determining an amount of energy in a single sub-signal of the multi-path profile if the length of the multi-path signal profile is less than a maximum number of taps of a single adaptive equalizer; and operating two or more adaptive equalizers, computational resources of the two or more adaptive equalizers, and operational blocks interconnecting said two or more adaptive equalizers according to said attributes of the multi-path signal profile. The closest prior art, Ueda (US 5,644,597) and co-pending application Mondragon-Torres et al. (US 7,561,618 B2) discloses a similar method but fail to disclose determining attributes of the multi-path signal profile, comprising determining an amount of energy in a single sub-signal of the multi-path profile if the length of the multi-path signal profile is less than a maximum number of taps of a single adaptive equalizer; and operating two or more adaptive equalizers, computational resources of the two or more adaptive equalizers, and operational blocks

interconnecting said two or more adaptive equalizers according to said attributes of the multi-path signal profile. This distinct feature has been added to claim 13, thus rendering claims 12-16 allowable.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SIU M. LEE whose telephone number is (571)270-1083. The examiner can normally be reached on Mon-Fri, 7:30-4:00 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Siu M Lee/

Examiner, Art Unit 2611

/CHIEH M FAN/
Supervisory Patent Examiner, Art Unit 2611